Supporting Information

Triply Degenerate Semimetal $PtBi_2$ as van der Waals Contacts in Two-Dimensional Transistor

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Note 1: Extraction of Schottky barrier from Arrhenius plot

The Schottky barrier height in this study was determined using a thermionic emission model, represented by the equation:

$$I_{ds} = A_{2D}^{*} \exp\left(-\frac{\phi_B}{k_B T}\right)\left[1 - \exp\left(-\frac{V_{ds}}{k_B T}\right)\right] \quad (1)$$

Where $A_{2D}^{*} = \frac{q\left(8\Pi {k_B}^3 m^3\right)^{0.5}}{h^2}$, h is the Planck constant for a 2D system, m is the electron effective mass, T is the temperature, k_B is Boltzmann's constant, q is the elementary charge, and ϕ_B is the effective contact barrier height for a given gate-source voltage (VGS). For 2D TMD semiconductors, when V_{ds} is much greater than k_B, equation (1) simplifies to:

$$\ln(I_{ds}/T^{1.5}) = \frac{-\Phi_B}{k_B T} + c \quad (2)$$

where c is a constant. Here, Φ_B is the extracted Schottky barrier for a certain VGS. To accurately characterize the thermionic emission at the metal-semiconductor interface, the Schottky barrier under a flat-band gate voltage ($V_{gs} = V_{FB}$) is typically used. Below the flat-band voltage ($V_{gs} < V_{FB}$), the device operates in the subthreshold regime, where channel resistance primarily governs the device conduction. Above the

flat-band voltage ($V_{gs} > V_{FB}$), the semiconductor beneath the contact region becomes highly doped, and a superimposed tunneling current reduces the extracted Φ_B. Theoretically, Φ_B exhibits a linear relationship with V_{gs} in the subthreshold regime ($V_{gs} < V_{FB}$) and transitions to a sublinear relationship ($V_{gs} > V_{FB}$). The V_{FB} and its corresponding flat-band Φ_B are accurately determined from the inflection point.

Note 2: Whole van der Waals (vdW) transfer

The vdW transfer process is shown in **Figure S1**. Both $PtBi_2$ and TMDs flakes were mechanical exfoliated from bulk crystal and then transfer onto the top surface of polydimethylsiloxane (PDMS). Then these material flakes as well as the Au electrodes were grabbed by polypropylene carbonate (PPC) with heating at 43 ℃. TMDs, $PtBi_2$ and Au electrodes then were released to the surface of substrate with 80 ℃ layer by layer to form a complicated vdW contact. This structure can provide a flatten, nondestructive interface between each layer, which is proved by SEM image **Figure S2**.

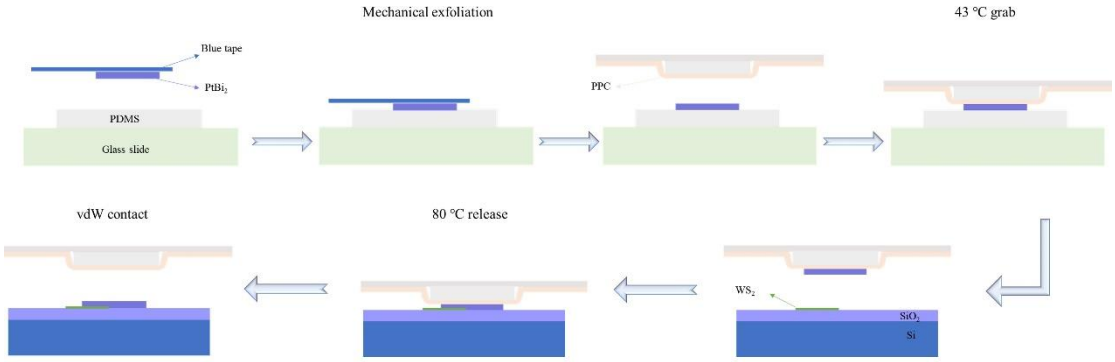

Figure S1. The schematic diagram of vdW transfer with PPC assistance.

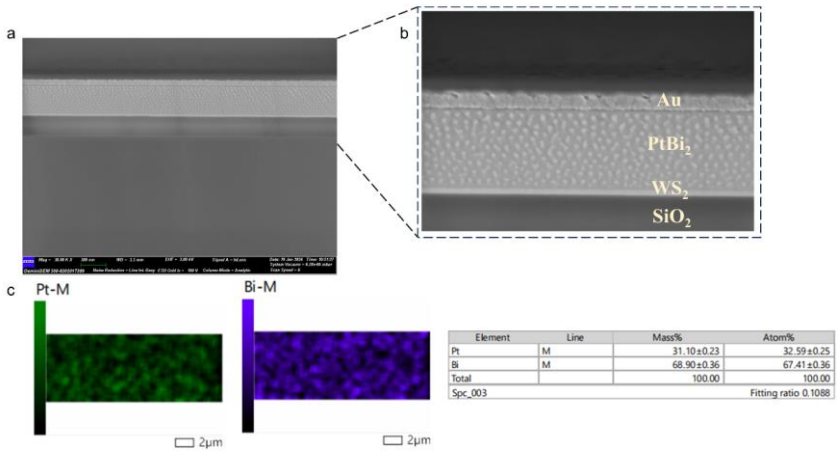

Figure S2. (a) The SEM image of the cross-section of Au/PtBi2/WS2/SiO2 multilayer. (b) Zoom-in SEM image of cross-section. There are no obvious defect or interstice between each layer. (c) EDS mapping and atom ratio calculation of PtBi2 flake.

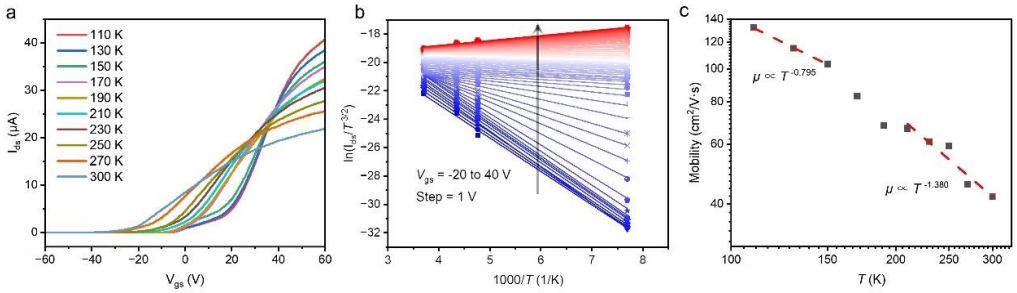

Figure S3. Temperature-dependent transport measurement (a) and related Arrhenius plot analysis (b) of device with thinner WS_2 nanoflakes. (c) Field-effect mobility as the function of temperature.

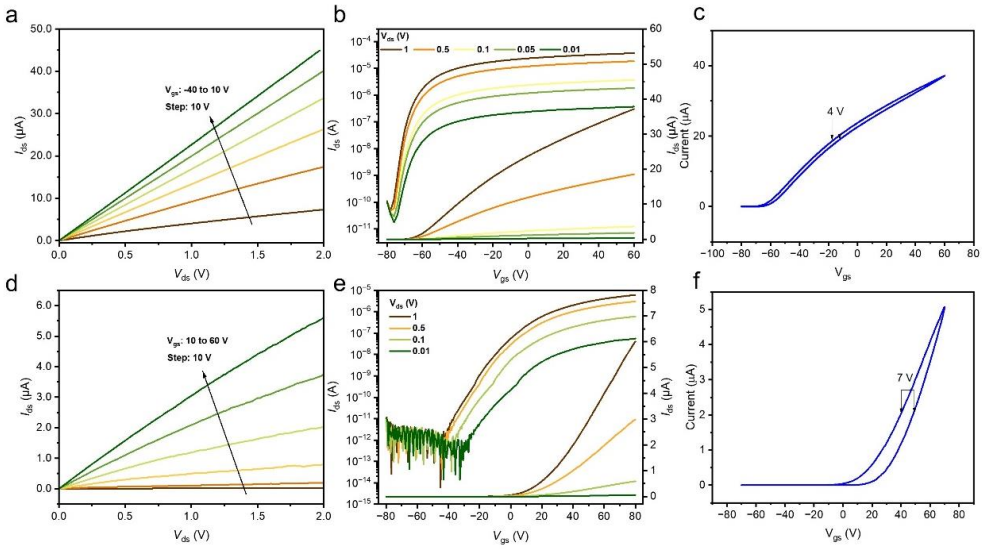

Figure S4. (a&d) Output and (b&e) transfer curve of transistor under room temperature for MoS_2 and WSe_2, respectively. The on-off ratio (>10^6) is determined from a semi-logarithmic plot of transfer while the mobility of 83.79 $cm^2V^{-1}s^{-1}$ for MoS_2 and 33.12 $cm^2V^{-1}s^{-1}$ for WSe_2 is obtained. (c&f) Transfer loop of MoS_2 and WSe_2, respectively.

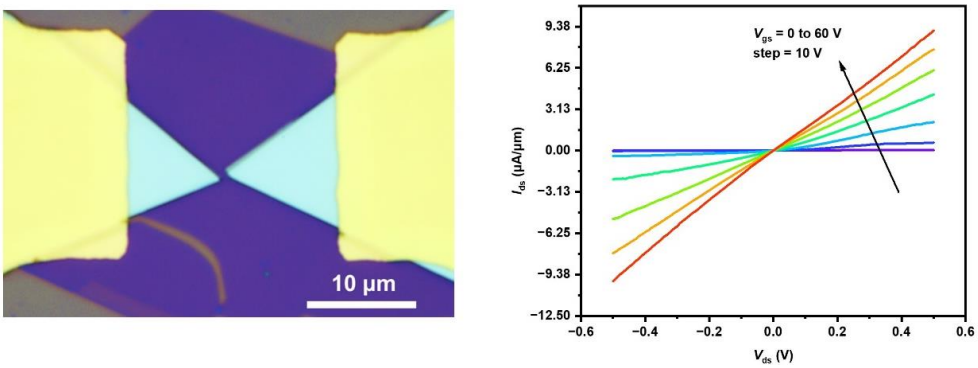

Figure S5. The output measurement of short-channel transistor under room temperature. Short-channel transistor also exist a linear output behavior.