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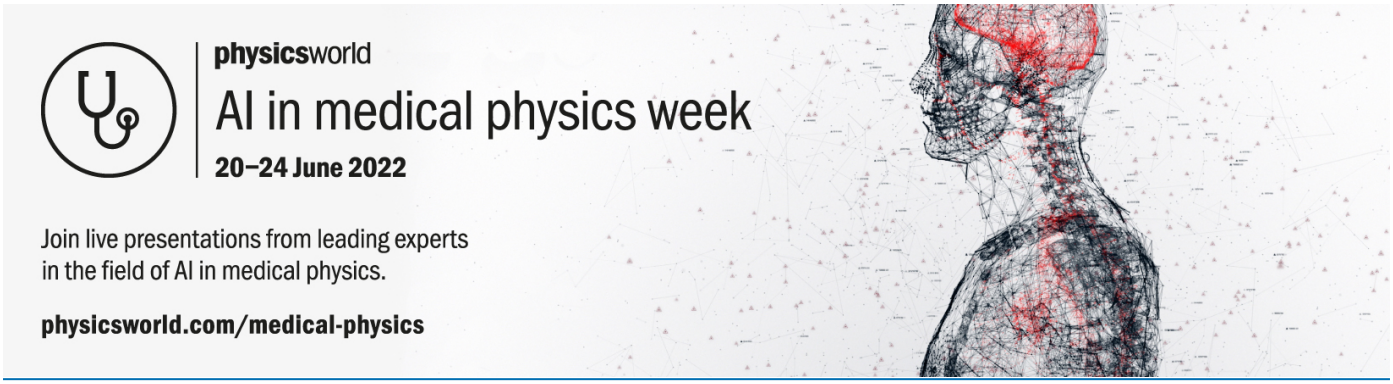

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Ultrafast flash memory with large self-rectifying ratio based on atomically thin MoS_2-channel transistor

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Abstract

Flash memory with high operation speed and stable retention performance is in great demand to meet the requirements of big data. In addition, the realisation of ultrafast flash memory with novel functions offers a means of combining heterogeneous components into a homogeneous device without considering impedance matching. This report proposes a 20 ns programme flash memory with 10^8 self-rectifying ratios based on a 0.65 nm-thick MoS_2-channel transistor. A high-quality van der Waals heterojunction with a sharp interface is formed between the Cr/Au metal floating layer and h-BN tunnelling layer. In addition, the large rectification ratio and low ideality factor ($n = 1.13$) facilitate the application of the MoS_2-channel flash memory as a bit-line select transistor. Finally, owing to the ultralow MoS_2/h-BN heterojunction capacitance (50 fF), the memory device exhibits superior performance as a high-frequency (up to 1 MHz) sine signal rectifier. These results pave the way toward the potential utilisation of multifunctional memory devices in ultrafast two-dimensional NAND-flash applications.

Supplementary material for this article is available online

Keywords: ultra-fast flash memory, metal floating gate, atomic sharp interface, atomic thin channel, self-rectification transistor, high-frequency rectifier

1. Introduction

Memory devices play an important role in modern electronic information technology, being widely used in computers and electronic devices. In the past few decades, numerous memory devices such as static random-access memory, dynamic random-access memory, and non-volatile flash memory have been developed. Among them, flash memory is extensively used as an information-storage device owing to its multibit per cell storage property, low power consumption, and stable retention capability. In traditional flash memory, the floating gate and conducting channel are usually based on polysilicon, whereas the blocking layer and tunnelling barrier are composed of silicon oxide [1, 2]. Given the explosive growth of data generated every year, the dimensions of memory will

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Future perspectives
Two-dimensional (2D) flash memory based on a 0.65 nm-thick MoS_2-channel transistor has shown superior performances in terms of higher programming/erasing speed and lower power consumption, which is attractive in future semiconductor architecture. However, flash memory does not function as a standalone system; it consists of word-line, bit-line, select transistor, peripheral circuit, and so on. The ability to combine the ultrafast flash memory with heterogeneous components into a homogeneous device is attractive, since it offers an avenue to integrate 2D devices into silicon industry without considering impedance matching. In addition, state-of-the-art 2D flash memories are mainly based on exfoliation method, and their operating voltage is relatively high, which is not suitable for industrialization and unwanted for low power applications. Much work deserves to be studied in depth, such as wafer-scale fabrication 2D flash memory arrays, layer-by-layer stacking 2D memory devices for 3D integrating, the reduction in operating voltage, *et al*. All these are necessary elements for lab-to-fab applications.

continue to shrink to achieve higher packing density and higher performance. However, the dimensions of memory will finally reach their physical limit, where charge leakage occurs when the Si layer is below a certain thickness, which degrades the retention performance [3, 4]. In addition, the operation speed remains a bottleneck in the current memory industry.

The pursuit of high-performance non-volatile flash memory devices with fast operation and stable retention has motivated researchers to seek new solutions. The continuous study of two-dimensional (2D) materials offers a possible avenue for realising this objective. The most attractive features of 2D materials are the dangling bonds that are free on their surfaces, their atomic crystallinity in a single layer, and their ability to be adhered to one another by the van der Waals force [5–7], offering an attractive platform for novel 2D electronic devices on the atomic scale. Accordingly, many successful attempts have been made to use 2D materials and their heterostructures to improve memory performance [8–16]. For example, the van der Waals MoS_2/h-BN/multilayer graphene (MLG) heterostructure [13] and van der Waals InSe/h-BN/MLG heterostructure [14] based flash memory have been proven to enable a 20 ns programming/erasing speed. Other van der Waals heterostructures, such as PtS_2/h-BN/Grephene [15] and ReS_2/h-BN/Grephene [16] have been demonstrated to have multibit optical memory or multilevel flash memory capabilities. Among these 2D material-based memory devices, h-BN is usually chosen as the tunnelling insulator, whereas MLG acts as the floating layer. The crystalline nature of h-BN presents a defect-free tunnelling layer. In addition, the van der Waals h-BN/MLG heterostructure manifests a sharp interface immune to the interfacial dangling bonds. All of these merits are essential for high-performance 2D memory devices.

The floating layer is anticipated to be the other important constituent in non-volatile memory devices because it determines the charge storage capacity and endurance/retention operation. For traditional non-volatile memory devices other than polycrystalline Si [1], high-k dielectric materials such as HfO_2 [17–19], TaN [20], organic films [21, 22], and metallic metal (Au, Pt) nanoparticles or nanoclusters [23–25] have also been used as floating layers to store and erase charge. Among them, metallic nanocrystal floating layers have several advantages because of their high trapping states, stable retention, and larger memory windows [26]. In addition, compared with the MLG floating layer (work function of ∼4.6 eV) [14], the large work functions of Au (5.1 eV) and Pt (5.7 eV) as metal floating gates create a deeper potential wall between the blocking and tunnelling layers, ensuring less charge leakage and higher stability. Furthermore, a recent report proved that the direct transfer of 2D materials onto a well-deposited metal film could also form an ideal van der Waals contact [6]. Thus, combining 2D materials with a metallic floating gate may offer an alternative means of fabricating a new flash memory with advanced device performance.

This report proposes an ultrafast flash memory based on an atomically thin MoS_2-channel transistor. This memory device differs from any developed previously, as it is using Cr/Au metal film as a floating layer. Despite using an h-BN dielectric insulating layer, the h-BN/(Cr/Au) heterolayer was also high quality stacked with an atomically sharp interface. In addition, the transistor as flash memory manifests a 1000 s endurance time and 20 ns programming speed, which is as fast as those recently reported. Through work function modulation, the transistor also exhibits a unique reverse rectification property with a maximum on/off ratio of 10^8 and a diode-like ideality factor (n) of 1.13. Accordingly, the transistor can function as an ultrafast flash memory and a bit-line select transistor. Finally, owing to the atomically thin MoS_2 channel (0.65 nm) and low capacitance ($C \sim 50$ fF), the memory device demonstrates the potential for application as a high-frequency half-wave rectifier, enabling the 1 MHz sine voltage to be transformed into a half-wave sine signal.

2. Results

2.1. Structural characteristics

Figure 1(a) shows the schematic crystal structure of the MoS_2-channel flash memory, in which the monolayer MoS_2 acts as a conduction channel, few-layer h-BN acts as a dielectric insulating layer, and the Cr/Au metal film serves as a floating gate with a transverse dimension larger than that of MoS_2. Supplementary figure S1 (available online at stacks.iop.org/MF/1/025301/mmedia) provides the corresponding optical microscopy images of each fabrication step. Firstly, the patterned 5 nm Cr/15 nm Au with sizes of 30 μm was patterned and pre-deposited onto a heavily doped p-type SiO_2/Si substrate with a SiO_2 thickness of 300 nm. Subsequently, mechanically exfoliated few layers of h-BN and a monolayer of MoS_2 were transferred onto the upper surface of the Cr/Au metal film in order of precedence to form the MoS_2/h-BN/(Cr/Au) van der Waals heterostructure (figures S1(a) and (b)). Finally, Cr/Au metals with thicknesses of 5 nm/30 nm were patterned and deposited to form the prototype memory device, as shown in figures 1(b) and S1(c).

Firstly, we characterised the stacking quality of the MoS_2/h-BN/(Cr/Au) van der Waals heterostructure using transmission electron microscopy (TEM). Figure 1(c) presents

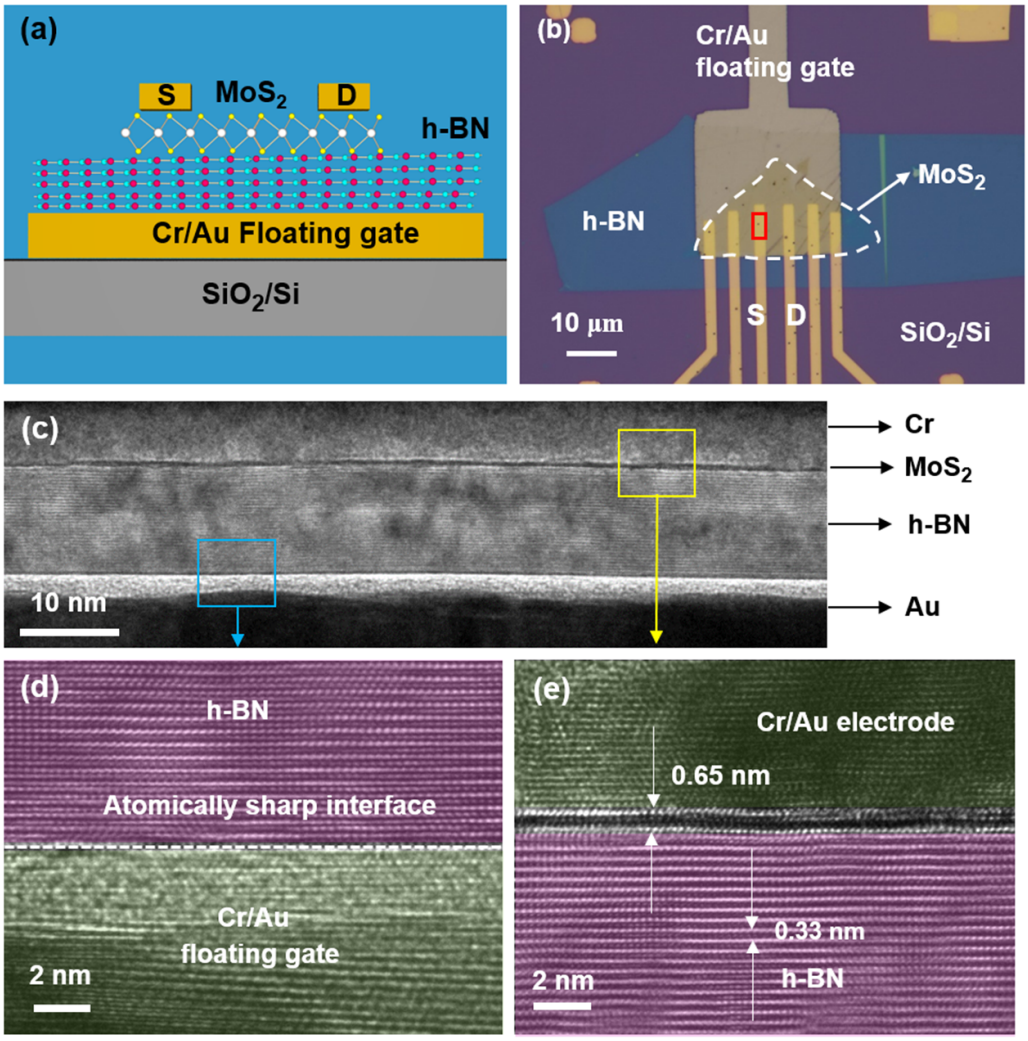

Figure 1. Structural characteristics of the non-volatile flash memory based on the h-BN/MoS_2 van der Waals heterostructure. (a) Schematic crystal structure of the flash memory with monolayer MoS_2 as a conduction channel, a few layers of h-BN as a tunnelling layer, and Cr/Au metal film as a floating gate. The floating layer is sandwiched between the h-BN and SiO_2/Si substrate. (b) Optical microscope image of the MoS_2-channel flash memory, where each layer is formed by the van der Waals force and the scale bar is 10 μm. (c) Cross-sectional transmission electron microscopy (TEM) image of the MoS_2/h-BN/(Cr/Au) heterostructure obtained from the red rectangular region in (b), where each layer can be observed clearly. (d) High-resolution-TEM (HRTEM) image of the selected blue area in (c), which proves the crystalline nature of the h-BN layer and high quality of the h-BN/(Cr/Au) heterostructure with an atomically sharp interface. (e) HRTEM image of the MoS_2/h-BN heterostructure from the selected yellow area in (c), proving that the 0.65 nm-thick MoS_2-channel has a sharp interface and defect-free metal contact.

a cross-sectional TEM image of the MoS_2/h-BN/(Cr/Au) heterostructure, obtained from the red rectangular region in figure 1(b). In the TEM image (figure 1(c)), each layer of the heterostructure can be clearly distinguished, and the h-BN layer thickness is 10.6 nm. According to the magnified view (the selected blue area in figure 1(c)) in figure 1(d), there is a sharp interface between the Cr/Au floating layer and h-BN insulating layer, proving that the h-BN/(Cr/Au) heterostructure can be stacked by van der Waals forces with high quality. Figure 1(e) provides a high-resolution TEM (HRTEM) image of the MoS_2/h-BN heterostructure corresponding to the yellow-box region in figure 1(c), demonstrating the crystalline nature of each material, atomically sharp interface, and monolayer MoS_2 channel with a thickness of 0.65 nm. In addition, no obvious defects are observed at the interface of the Cr/Au metal electrode. A high-quality van der Waals heterostructure without interface defects is essential to eliminate interfacial Fermi level pinning effects and to improve device performance.

2.2. *Output and transfer characteristics*

Before studying the electrical performance of the MoS_2-channel flash memory, we prepared a MoS_2-channel field-effect transistor (FET) and examined its electrical properties. The MoS_2-channel FET was based on the MoS_2/h-BN heterostructure directly transferred onto a SiO_2/Si substrate, and figure S2 shows the corresponding optical microscope

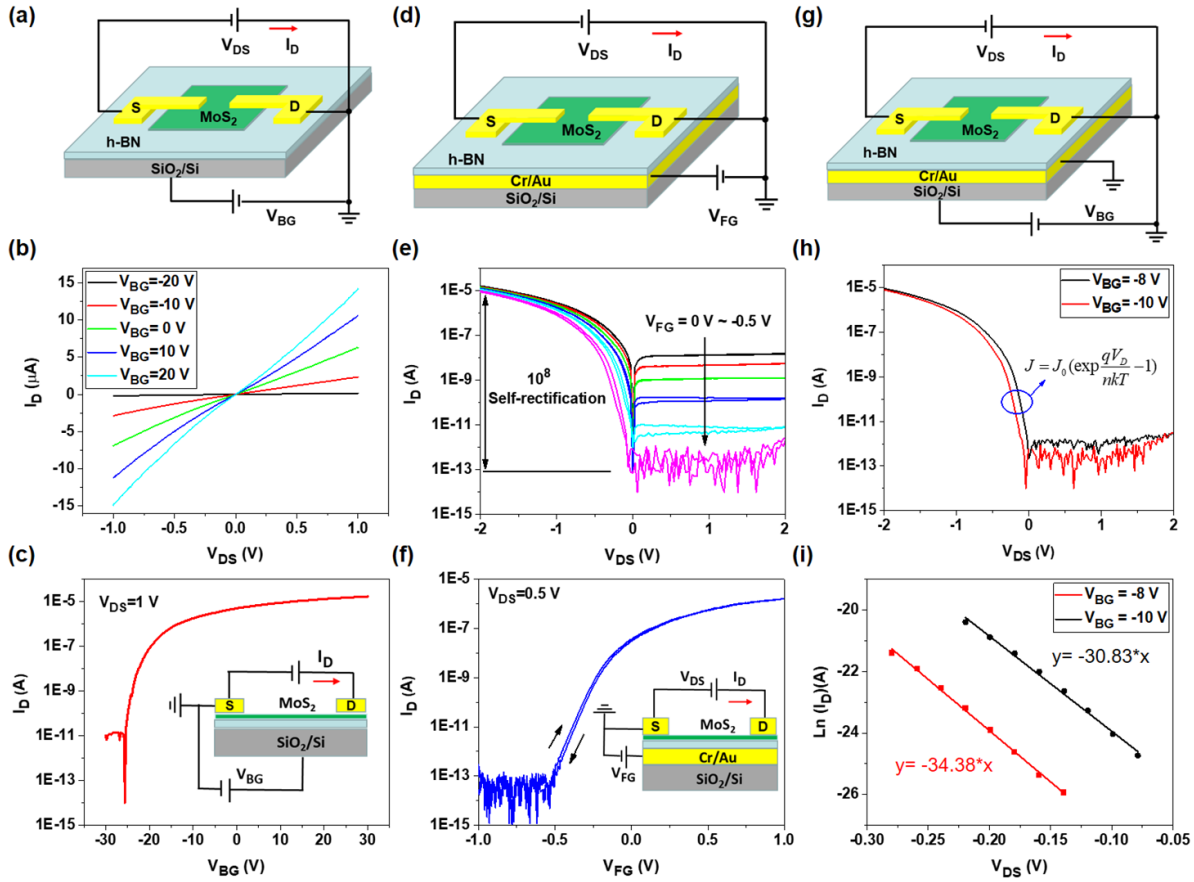

Figure 2. Output and transfer characteristics of MoS_2-channel transistors with different device structures and electrical connections. (a) Schematic of the electrical connections of the MoS_2-channel field-effect transistor (FET) directly transferred onto the h-BN with SiO_2/Si substrate as the back gate (V_{BG}). (b) Output characteristics of the MoS_2-channel FET under different V_{BG}, where the drain current (I_D) increases linearly increasing drain-to-source voltage (V_{DS}), proving Ohmic-like contact. (c) Transfer curves of the MoS_2-channel FET, demonstrating the existence of an n-type conductive channel. Inset shows a cross-sectional view of the electrical connection. (d) Schematic of the electrical connection of the MoS_2-channel transistor with Cr/Au metal film as gate electrode (V_{FG}). (e) Output characteristics of the transistor in (d) under different V_{FG}, showing reverse self-rectification behaviour with an on/off ratio of $\sim 10^8$. (f) Double-swept transfer curve of the transistor. No obvious hysteresis is seen from the curve, suggests the existence of a sharp MoS_2/h-BN/Au heterostructure interface. (g) Schematic of the electrical connections of the MoS_2-channel transistor connected with V_{BG} while grounding V_{FG}. (h) Output characteristics of the transistor in (g) at $V_{BG} = -8$ V and -10 V. The output curves behaved as a reverse p-n junction diode with an ideality factor of ~ 1.13. (i) The $\ln(I_D) \sim V_{DS}$ curves acquired from the blue circle region in (h), where the fitted linear slopes are -30.83 and -34.38.

images of each fabrication step. Figure 2(a) provides a schematic of the electrical connections of the MoS_2-channel FET with a Cr/Au (5 nm/30 nm) metal electrode, where the gate voltage (V_{BG}) was applied at the back of the SiO_2/Si substrate. Figures 2(b) and S3 show the typical output curves (drain current, I_D, versus drain-to-source voltage, V_{DS}) of the MoS_2-channel FET. The linear increase in I_D as a function of V_{DS} proves the existence of good Ohmic-like contact between the MoS_2 channel and Cr/Au metal electrode [27–29]. In addition, according to the transfer curves (I_D versus V_{BG}) in figure 2(c), the MoS_2 conduction channel exhibits a strong n-type behaviour with a threshold voltage (V_{TH}) of ~ -25 V. Thus, a high-performance MoS_2-channel FET with approximate Ohmic contact and high injection current (~ 15 μA at $V_{DS} = \pm 1$ V and $V_{BG} = -20$ V) was demonstrated using this method.

Then, the output and transfer characteristics from Cr/Au metal mediated MoS_2-channel transistor was studied. In contrast to the MoS_2-channel FET depicted in figure 2(a), an additional Cr/Au (5 nm/15 nm) metal film was deposited between the SiO_2 block layer and h-BN tunnelling layer. Figure 2(d) shows a schematic of the electrical connection of the transistor when the gate voltage applied at Cr/Au metal (V_{FG}). A unidirectional rectification characteristic is observed (figures 2(e) and S4) rather than a linear output characteristic (figure 2(b)). The more negative the V_{FG} applied, the larger the reverse reaction ratio obtained. The maximum reverse rectification ratio reaches $\sim 10^8$ at $V_{DS} = \pm 2$ V and $V_{FG} = -0.5$ V. This value is larger than most reported for 2D material-based Schottky diodes [30, 31], backward diodes [32–34], and van der Waals p-n heterojunction diodes [35, 36]. Figure 2(f) shows the transfer characteristics of the transistor at $V_{DS} = 0.5$ V. When V_{FG}

is swept between −1 V and 1 V, I_D increases with increasing V_{FG}, proving the n-type behaviour of the MoS_2 channel. In addition, due to ultrathin nature of the h-BN (∼10.6 nm) insulating layer, V_{TH} could be further reduced to ∼−0.5 V. No obvious hysteresis appears in the curve, suggesting the high quality of the heterostructure interface with negligible trap states.

It is notable that the Cr/Au metal electrodes in figures 2(a) and (d) were fabricated using the same deposition facility. However, the different output curves in figures 2(b) and (e) suggest that the introduction of a metal film would result in unusual electrical performance. Similar results were also observed when we grounded V_{FG} and applied V_{BG}, the electrical connection is schematically shown in figure 2(g). Figure S5 depicts the corresponding I_D–V_{DS} curves at V_{BG} ranging from 0 V to −10 V, while figure 2(h) illustrates the output curves obtained from figure S5(b) at $V_{BG} = -8$ V and −10 V, respectively. A maximum rectification ratio of $\sim 10^8$ occurs at $V_{BG} = -10$ V. The reverse rectification is mainly attributed to the formation of two asymmetric Schottky contacts at the drain and source electrodes; the work mechanism had been explained in our previous work [37] and reported by other research groups [38, 39]. The reverse rectification behaviour can be further explained using the energy-band diagrams in figures S6 and S7. When a negative V_{FG} or V_{BG} is applied to the floating layer or SiO_2/Si substrate (figure S7(a)), a downward electric field is formed between the drain and gate. This situation results in the depletion of the MoS_2-channel at the drain and source sides, changing from symmetric contact barrier (figure S7(a)) to asymmetric Schottky contact (figure S7(b)). We define $q\phi_1$ as the barrier height at the drain side and $q\phi_2$ as the barrier height at the source side, which satisfy $q\phi_1 > q\phi_2$. For $V_{FG} < 0$ V and $V_{DS} > 0$ V (figure S7(c)), the more negative the V_{FG} or V_{BG} value applied, the higher the $q\phi_1$ value achieved, which in turn decreases the forward I_D and increases the on/off ratio. For $V_{FG} < 0$ V and $V_{DS} < 0$ V (figure S7(d)), the Schottky barrier at the drain side is a reverse bias, whereas the barrier at the source side is a forward bias. However, the voltage does not change the barrier height of $q\phi_1$, and the exponential increase in I_D may be attributed to the image force-induced barrier-lowering effects [39]; that is, the Schottky barrier height at the drain side decreases when the forcing electrode is in the reverse bias condition ($V_{DS} < 0$ V).

The MoS_2-channel memory device behaved as a reverse p-n junction diode. The equation is as follows [40]:

$$J = J_0 \left(\exp \frac{qV_D}{nkT} - 1 \right)$$

where J represents the channel current, J_0 represents the reverse saturation current, n represents the ideality factor (commonly between 1 and 2), V_D represents the applied voltage, and k and T represent Boltzmann's constant and the temperature in Kelvin, respectively. When $V_D > {}^{3kT}/_{e}$ (∼0.08 V) [41], the equation can be simplified as

$$J = J_0 \left(\exp \frac{qV_D}{nkT} \right).$$

Accordingly, figure 2(i) plots the $\ln(I_D)$–V_{DS} curve in the V_{DS} range from −0.08 V to −0.28 V (green circle region in figure 2(h)), showing a linear increase. The slopes of the linear fitted curves are −30.83 and −34.38; thus, the calculated n values at room temperature ($T = 298$ K) are 1.26 ($V_{BG} = -8$ V) and 1.13 ($V_{BG} = -10$ V), respectively. These values are very close to that of the ideal p-n diode. This phenomenon is very interesting because it can combine the low onset voltage of the Schottky diode and the large on/off ratio of the p-n junction diode. These merits enable the usage of this device as a bit-line select transistor in NAND-flash applications [42].

Figure 3(a) depicts the electrical connections of the MoS_2-channel transistor function as flash memory when I_D is controlled by V_{BG} without grounding V_{FG}. I_D was measured as a function of V_{DS} as V_{BG} was increased from −10 V to 10 V in 5 V steps. As seen in figure 3(b), for $V_{BG} = -10$ V (black curve), I_D gradually decreases to 10^{-12} A. Under this condition, the MoS_2 channel is completely switched off, and the memory device is in a high-resistance state (low state). However, when V_{BG} increases to −5 V (red curve), the maximum I_D at $V_{DS} = -2$ V is approximately 10^{-5} A. The drain current seldom changes even when V_{BG} increases further from −5 V to 10 V. Under this condition, the MoS_2 channel is completely switched on, and the memory device is in a low-resistance state (high state). Similar results are also evident in figure S8 when V_{BG} changes from 0 V to −20 V in −5 V steps. Only two states are observed (i.e. the 'low-resistance state' at $V_{BG} = 0$ V and the 'high-resistance state' at $V_{BG} < 0$ V), which may be because the MoS_2-channel electrons tunnel through the h-BN layer and accumulate at the Cr/Au metal floating layer or the stored electrons at the floating layer return to the MoS_2 channel. The stored or depleted electrons weaken or strengthen the electric field strength of V_{BG}.

Figure 3(c) shows the dual-sweep transfer curves of the MoS_2-channel transistor (corresponds to figure 1(b)). Numerous transfer curves with a maximum V_{BG} increasing from 5 V to 15 V in 2.5 V steps are apparent, and an obvious memory window exists even when V_{FG} doubles from −5 V to 5 V. In addition, the memory window width (ΔV, figure S9) proportionally increases with increasing V_{BG}, and the maximum memory window width reaches 27.8 V when V_{BG} doubles from −15 V to 15 V (figure 3(d)). Similar results are observed for other MoS_2-channel memory devices (figure S10). In the dual-swept transfer curves of the memory device acquired by sweeping V_{BG} back and forth at $V_{DS} = 0.1$ V, a memory window width of ∼41.8 V is observed when V_{BG} changes from −25 V to 25 V. The large memory window is mainly attributed to the high-density states of the metal floating layer, facilitating potential applications in high-performance flash memory.

2.3. *Ultrafast flash memory performances*

We then used an energy diagram to elucidate the working mechanism of the memory device. When a positive V_{BG} pulse (25 V, 20 ns) was applied at the back of the SiO_2/Si substrate, electrons from the MoS_2-channel began tunnelling through the h-BN insulating layer and accumulated at the Cr/Au floating layer, corresponding to the programme

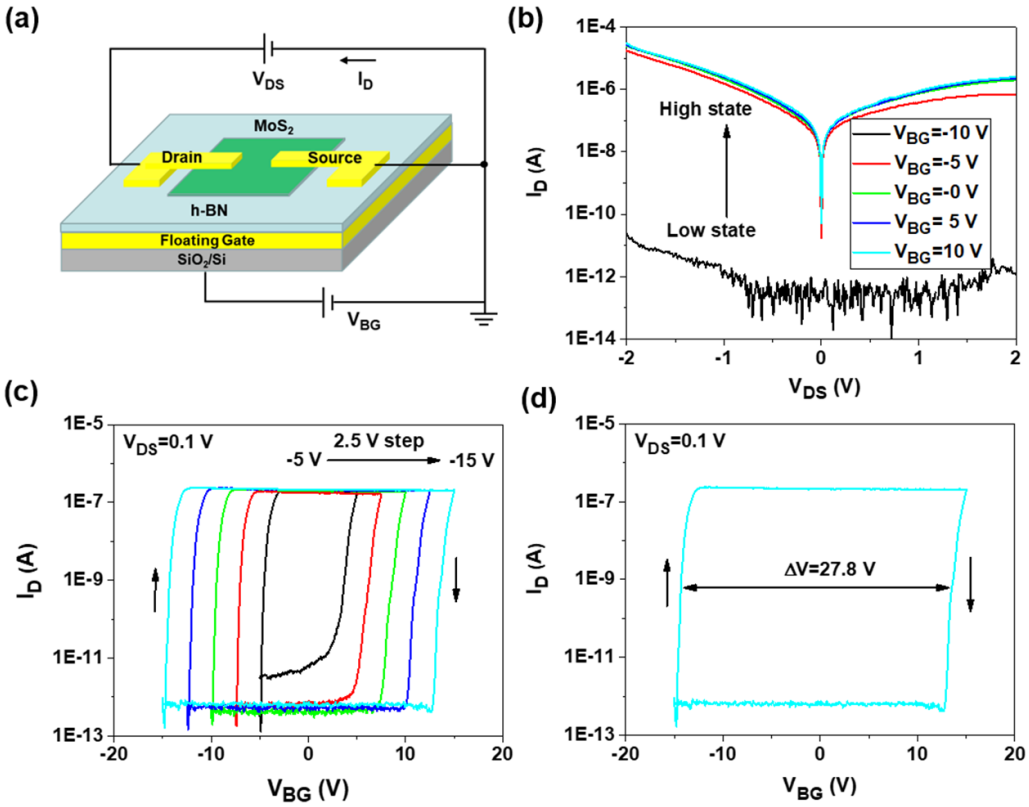

Figure 3. Output and transfer characteristics of the MoS_2-channel flash memory. (a) Schematic of the electrical connections of the memory device when V_{BG} is applied at the back of the SiO_2/Si substrate without grounding V_{FG}. (b) Output characteristics of the memory device at V_{BG} from −10 V to 10 V in 5 V steps, showing only two states (low and high states) regardless of the variation of V_{BG}. (c) Transfer curves of the memory device at $V_{DS} = 0.1$ V, where the memory window width increases with increasing V_{BG}. (d) Corresponding transfer curves of the memory device acquired from (c) with V_{BG} swept between −15 V and 15 V. The calculated memory window width is ∼27.8 V, suggesting that more electrons can be stored in the Cr/Au floating layer.

operations (figure 4(a)). The accumulated electrons were well stored in the floating layer, even when the applied V_{BG} pulse was removed, resulting in a low conductance of the MoS_2 channel, corresponding to the '0' state (figure 4(b)). However, when a negative V_{BG} pulse (−25 V, 20 ns) was applied to the substrate, the stored electrons in the floating layer began tunnelling back to the MoS_2 channel, which corresponds to the erase operation (figure 4(c)). After treatment with a −25 V, 20 ns V_{BG} pulse, the stored electrons in the floating layer were completely removed and the MoS_2 channel returned to its original state with high conductance, corresponding to the '1' state (figure 4(d)).

The typical programming/erasing operations of the proposed MoS_2-channel flash memory were experimentally investigated using 25 V/−25 V, 20 ns V_{BG} pulses. Figure S9(a) shows an optical microscopy image of the MoS_2-channel flash memory, and figure 4(e) schematically depicts the electrical connection of the measurement setup. The programming and erasing operations were performed by separately applying ±25 V, 20 ns V_{BG} pulses (figure 4(f)), whereas the readout operations were performed with V_{DS} fixed at 0.1 V. As seen from the curve, within a 250 s time period, the '0' and '1' states seldom change, indicating that the device can work as an ultrafast speed flash memory with a 20 ns operation speed. Figure 4(g) provides an example of flash memory performance analysis by characterising the transfer curves after treatment with different V_{BG} pulses. According to the optical microscope image in figure 1(b), the memory device contains a 0.65 nm-thick MoS_2 channel and a 10.6 nm-thick h-BN layer. Firstly, we applied a −25 V, 1 s V_{BG} pulse to erase the MoS_2 channel fully. Subsequently, the transfer curve of the memory device was measured (black line, figure 4(g)) with V_{TH} of approximately −6 V. After applying a 20 V, 50 ns pulse, V_{TH} is right-shifted to −4 V. However, when the pulse V_{BG} further increases to 25 V, V_{TH} is right-shifted to −3.3 V. V_{TH} gradually saturates when the pulse V_{BG} is larger than 25 V. The right shift of V_{TH} further proves that the electrons tunnel from the MoS_2 channel to the floating gate.

The endurance and retention characteristics are two key parameters for flash memory devices. Figure 4(h) depicts the retention property of the memory device with 10.6 nm-thick h-BN. Under this condition, the pulse voltage was fixed at 25 V, whereas the pulse width increased to 50 ns to tunnel the electrons fully. When a positive V_{BG} pulse was applied, the MoS_2 channel was driven to a low-conductance state, corresponding to the programme state, and vice versa. The retention time was as long as 1000 s, suggesting good stability of this memory device. It is worth mentioning that, the on current (erase state) has a slightly decrease within 1000 s retention time, this may be attribute to carrier recombination at

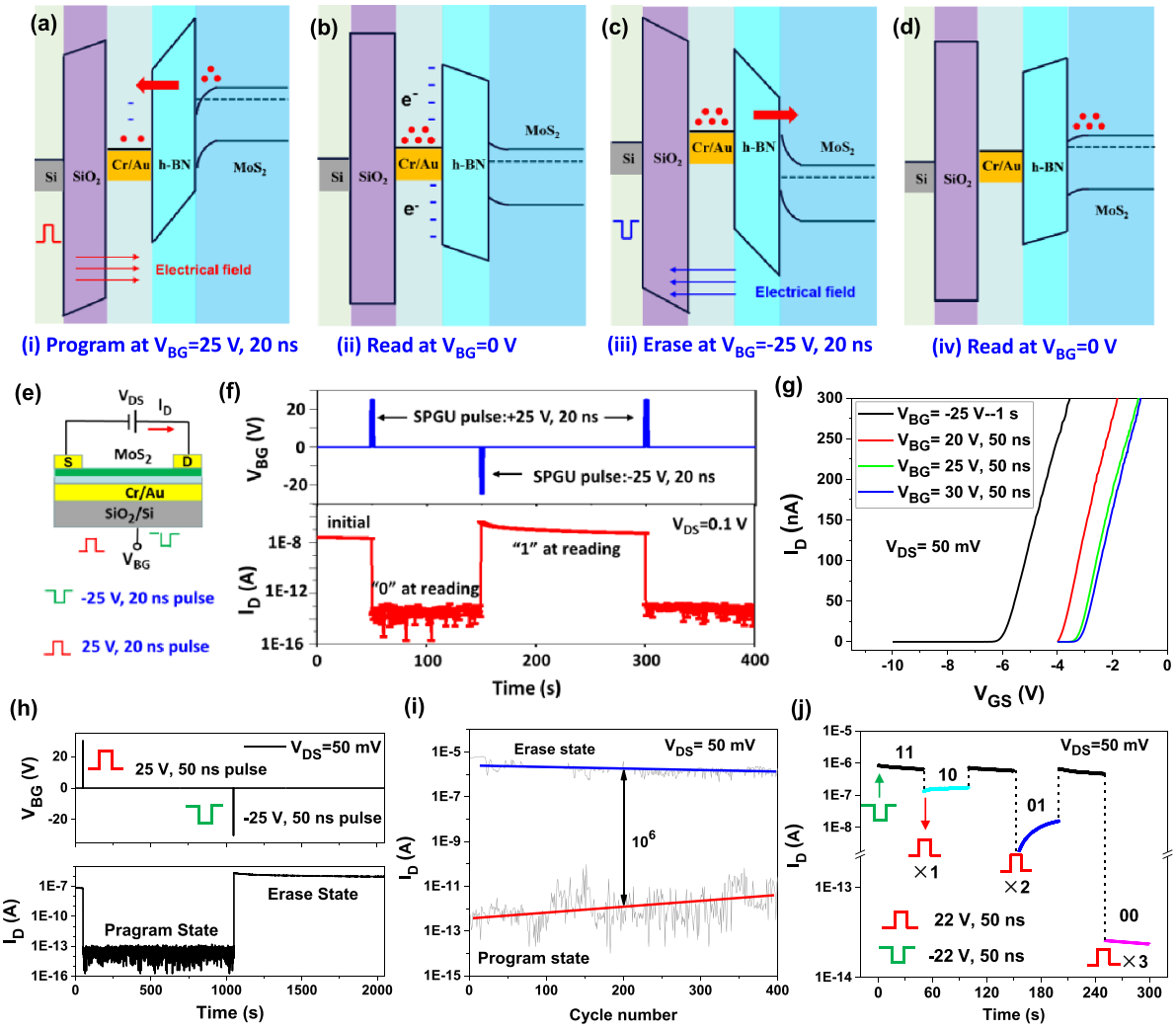

Figure 4. Programming and erasing performances of the MoS_2-channel flash memory. (a) Schematic energy-band diagrams of the memory device programmed after applying a 25 V, 20 ns V_{BG} pulse; (b) read at $V_{BG} = 0$ V; (c) erased with a $V_{BG} = -25$ V, 20 ns pulse; and (d) read at $V_{BG} = 0$ V. (e) Electrical connection of the memory device when a 20 ns, ± 25 V pulse was applied at the back of the SiO_2/Si substrate. (f) Time-resolved I_D change after applying periodic $+25$ V and -25 V, 20 ns V_{BG} pulses. I_D was measured at $V_{DS} = 0.1$ V. Within the time intervals, the '0' and '1' states seldom change, indicating ultrafast non-volatile memory. (g) Transfer curves of the MoS_2-channel flash memory before and after applying different positive pulses (20, 25, and 30 V; pulse duration 50 ns); the device shows a distinct rightward shift in the threshold voltage. (h) Retention characteristics of the MoS_2-channel flash memory with 10.6 nm-thick h-BN. V_{BG} is ± 25 V, 50 ns, and the device reveals stable retention up to 1000 s. (i) Endurance of the MoS_2-channel flash memory with ± 25 V, 1 μs pulses for 400 writing/erasing cycles. (i) Reproducible two-bit storage characteristics of the memory device. Under a certain voltage pulse (± 22 V, 50 ns), multilevel states are realised by increasing the number of pulses.

floating layer and insulator interface. In addition, according to the switching performance of the MoS_2-channel flash memory in figure S11, the two states are almost unchanged within the time sequence. The endurance characteristics (figure 4(i)) show an on/off ratio of up to 10^6 for 400 program/erase cycles. The number of program/erase cycles of our device may be low compared with those of non-volatile flash memory in CMOS technology (>10^4 cycles) [1, 43] and other 2D material-based memory devices (>2×10^3 cycles) [13, 14, 44], which may because of the use of active metal Cr in the Cr/Au floating layer. That is, the Cr atoms are easily oxidised to form Cr^{3+} cations under a voltage bias. Subsequently, the Cr^{3+} cations migrate into the h-BN insulating layer under a positive V_{BG} pulse, resulting in the formation of a conductive filament and destruction of the crystal structure of h-BN [45, 46]. We are confident that the endurance of the MoS_2-channel flash memory can be further improved if we choosing an inactive metal (Pd, or Pt) [45] as the floating layer or a new van der Waals dielectric material (Sb_2O_3, Bi_2SeO_5) [47, 48], which will be studied in the future.

Because the number of tunnelling electrons can be modulated by the pulse width and pulse voltage, figure 4(j) exemplifies the two-bit storage capabilities of the MoS_2-channel flash memory. Under a certain pulse voltage (± 22 V, 50 ns), the multilevel states ('11', '10', '01', and '00') are achieved by increasing the number of pulses. Overall, the MoS_2-channel transistor also has potential applications in multibit flash memory. It is worth mentioning that the main difference

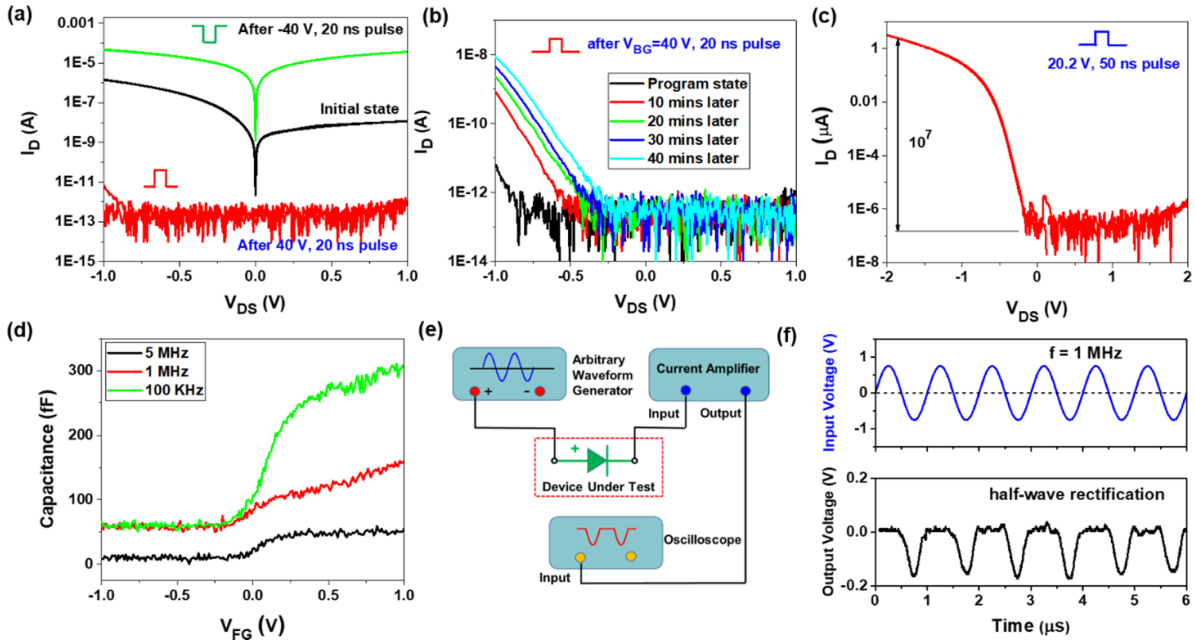

Figure 5. High-frequency sine single half-wave rectification property based on MoS_2-channel flash memory. (a) Output characteristics of the MoS_2-channel flash memory in the initial state (black curve), high-resistance state (red curve, treated with a 40 V, 20 ns V_{BG} pulse), and low-resistance state (green curve, treated with a −40 V, 20 ns V_{BG} pulse), respectively. (b) Endurance characteristics of the memory device after treatment with a 40 V, 20 ns V_{BG} pulse, where the output curves were separately measured in 10 min intervals. (c) Output characteristics of the MoS_2-channel flash memory after treatment with a −20.2 V, 50 ns V_{BG} pulse. Reverse rectification is observed with an on/off ratio of $\sim 10^7$. (d) Capacitance (C)–voltage (V_{FG}) characteristics of the memory device between the drain and floating layer at frequencies of 5 MHz, 1 MHz, and 100 KHz. (e) Schematic illustration of the half-wave rectifier setup, which consists of an arbitrary waveform generator, a current amplifier, and an oscilloscope. (f) Half-wave rectification characteristics of the MoS_2-channel transistor. After applying a 1 MHz input sine signal, the memory device output a perfect half-wave signal.

between our flash memory transistor and recently reported 2D material-based memory devices (i.e. van der Waals MoS_2/h-BN/MLG heterostructures [13], van der Waals InSe/h-BN/MLG heterostructures[14]) is the manner in which the floating gate is separately formed by the Cr/Au metal film and multilayer graphene. Owing to the large work function difference and work function engineering of the Cr/Au floating layer and MoS_2 channel, we observed the formation of two asymmetric Schottky contacts with the MoS_2 conduction channel rather than Ohmic-like contact (figure S3). Thus, the MoS_2-channel flash memory also exhibits a reverse self-rectification behaviour with an on/off ratio $>10^8$ and a p-n diode-like ideality factor as low as $\sim$1.13. This phenomenon is very interesting because the device could function not only as an ultrafast flash memory, but also as a potential application for a bit-line select transistor. Accordingly, the ultrafast flash memory and a selected transistor can be combined. If the switch on/off frequency of the selected transistor is as fast as that of the flash memory, the 2D material-based memory device would be attractive for 2D material-based NAND-flash applications. The switch on/off frequency can be characterised by its half-wave rectification performance, as shown in figure 5.

2.4. High-frequency half-wave rectification characteristics

Because the number of tunnelling electrons can be modulated by the pulse voltage, the output characteristics of the MoS_2-channel flash memory under different V_{BG} pulse conditions were studied. Figure S12(a) shows the schematic electric connections of the measurement setup, where the I_D–V_{DS} curves were separately measured under the initial conditions (without applying a V_{BG} pulse), after treatment with a negative V_{BG} pulse (−40 V, 20 ns), and after treatment with a positive V_{BG} pulse (40 V, 20 ns). Figure 5(a) depicts the corresponding output curves. Without applying a V_{BG} pulse (initial state), we observed a reverse drain current two orders of magnitude larger than the forward condition (black curve in figure 5(a)), in agreement with the results in figure 2(e). After applying a 40 V, 20 ns V_{BG} pulse (red curve in figure 5(a)), I_D seldom changes ($\sim 3 \times 10^{-13}$ A). Under these conditions, the tunnelling electrons are fully accumulated in the floating layer, resulting in MoS_2 channel switch-off. However, after applying a −40 V, 20 ns V_{BG} pulse, a symmetric I_D as a function of V_{DS} was obtained, and the maximum I_D at $V_{DS} = \pm 1$ V was $\sim$44 μA (green curve in figure 5(a)), eight orders of magnitude higher than that under the switch-off condition.

Figures 5(b) and S12(b) present the endurance performance of the MoS_2-channel flash memory after treatment with different V_{BG} pulses. The I_D–V_{DS} curves were separately measured in 10 min intervals. As seen from the curves, both the low-resistance state (figure S12(b)) and high-resistance state (figure 5(b)) can be retained for more than 30 min with little change, suggesting the good retention capability of the MoS_2-channel flash memory. The output curves of the same memory device were also studied by decreasing the V_{BG} pulse

voltage and increasing the pulse width. Figure S13(a) shows a schematic of the electrical connections of the memory device with variation from ±25 V to ±18 V, while the pulse width was fixed at 50 ns. With a ±25 V, 50 ns V_{BG} pulse (figure S13(b)), we obtained the same output curves as in figure 5(a). However, when the V_{BG} pulse decreased to 21 V (figure S13(c)) or below (figures S13(d) and (e)), the MoS_2-channel was unable to switch-off fully owing to the insufficient tunnelling process. Figure 5(c) depicts one output curve after treatment with a 20.2 V, 50 ns V_{BG} pulse, showing a reverse rectification property with an on/off ratio of up to 10^7, similar to the results in figure 2(e). Under this condition, only some of the electrons are capable of tunnelling through the h-BN layer. Thus, the reverse rectification behaviour can be realised either by a constant negative V_{FG} pulse (figure 2(e)) or a positive V_{BG} pulse (figure 5(c)).

Figure 5(d) shows the MoS_2/h-BN heterostructure capacitance (C) as a function of V_{FG} at different frequencies (f). The measurement was conducted when V_{FG} was applied between the floating gate and source electrode. A minimum C of 50 fF was obtained at $V_{FG} = 1$ V, $f = 5$ MHz. The ultralow heterojunction capacitance, together with the large on/off ratio, make the MoS_2-channel flash memory potentially usable as a high-frequency half-wave rectifier. Figure 5(e) shows a schematic of the measurement setup, which contains an arbitrary waveform generator (AWG) to produce a high-frequency sine or square voltage signal, a current amplifier to transfer the current signal to the voltage signal, and an oscilloscope to display the output voltage signal. During the measurement, the output sine voltage signal from the AWG was connected to the drain electrode, whereas the source electrode was connected to the input port of the current amplifier. Figure 5(f) depicts the half-wave rectification characteristics of the MoS_2-channel flash memory after treatment with a 20.2 V, 50 ns pulse (figure 5(c)). Owing to its reverse rectification property, only the reverse half-wave sine signal can pass through the MoS_2-channel. The blue line in figure 5(f) presents the input sine voltage signal with a peak-to-peak value of 0.75 V and frequency of 1 MHz. The output curves (black line in figure 5(f)) display an ideal half-wave sine waveform. Similar results are observed in figure S14, where the half-wave rectification limit reaches 3 MHz. It is worth mentioning that the half-wave rectification frequency is three orders of magnitude higher than that of the commercial p-n junction diode (∼1 kHz, figure S15(b)) with a heterojunction capacitance of ∼120 pF at $f = 1$ MHz (figure S15(d)). The high rectification frequency may be due to the ultralow junction capacitance of the MoS_2-channel flash memory induced by the ultrathin heterojunction with an atomically sharp interface, paving the way toward the realisation of a low-power, high-frequency sine signal rectifier.

3. Conclusions

In summary, we demonstrated the performance of an ultrafast flash memory with an atomically thin channel transistor. The memory device is composed of a monolayer MoS_2 channel, a few layers of h-BN, and a Cr/Au metal floating gate. Due to the high-density charge states and work function engineering of the metallic floating gate, the flash memory manifests a larger memory window width of 27.8 V when it is double-swept from −15 V to 15 V, achieves ultrafast programming/erasing speed down to 20 ns, reveals stable retention up to 1000 s, and endures over 400 cycles. Though the number of program/erase cycles of our device may be low, the memory performance can be improved by choosing an inactive metal as the floating layer or using other van der Waals dielectric material. In addition, the MoS_2-channel flash memory demonstrates a unique self-rectifying behaviour with an on/off ratio larger than 10^8, which is very interesting and can enable use as a bit-line select transistor in NAND flashes. Furthermore, the large on/off ratio and low junction capacitance (50 fF) facilitate the potential application of this device as a high-frequency (>1 MHz) half-wave rectifier. These results pave the way toward the realisation of ultrafast flash memory with novel functionality in modern semiconductor architecture.

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